
Design for Manufacturability and Yield for Nano-Scale CMOS

Charles C. Chiang

layout for Manufacturability and Yield for Nano-Scale CMOS walks the reader via the entire facets of manufacturability and yield in a nano-CMOS technique and the way to handle each one point on the right layout step beginning with the layout and format of ordinary cells and the way to yield-grade libraries for severe zone and lithography artifacts via position and route, CMP version established simulation and dummy-fill insertion, masks planning, simulation and manufacturing, and during statistical Design for Manufacturability and Yield for Nano-Scale CMOS layout and statistical timing closure of the design. It signals the clothier to the pitfalls to monitor for and to the great practices that could improve a layout s manufacturability and yield. This ebook is a needs to learn ebook the intense practising IC fashion designer and a very good primer for any graduate scholar rationale on having a occupation in IC layout or in EDA software development."

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